TS7029N - 100W CW, 631W Peak GaN RF Switch

1.0 Features

- Low TX insertion loss: 0.40dB @ 800MHz
- High isolation: 50dB @ 800MHz
- 631W Peak Power Handling
- Versatile 2.6-5.5V power supply
- Operating frequency: 700MHz to 2.7GHz

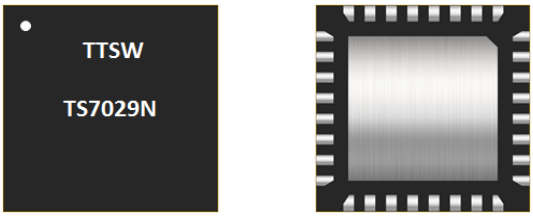


Figure 1 Device Image
(32 Pin 5×5×0.85mm³ QFN Package)

2.0 Applications

- Cellular infrastructure
- Small cells
- Macrocells
- ADS-B, IFF Systems

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS7029N is an asymmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high power switching applications. With a simple broadband match, the TS7029N can cover 700M to 2.7GHz bandwidth and provide low insertion loss, high isolation and high linearity within a small package size. TS7029N is an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7029N is packaged into a compact Quad Flat No lead (QFN) 5x5mm 32 leads plastic package.

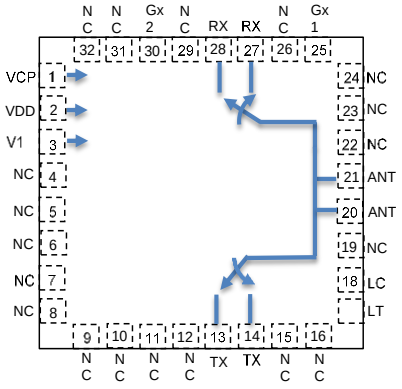


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS7029N	32 Pin 5.0×5.0×0.85mm³ QFN	Tape and Reel	1000	13” (330mm)	18mm	TS7029NMTRPBF
Evaluation Board						TS7029N-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
2	VDD	DC power supply
3	V1	Switch control input 1
4,5,6,7,8,9,10,11,16,23,24,31,32	NC	No internal connection, can be grounded
12,15,19, 22,26,29	NC	No internal connection. Must be left Open
13,14	TX	TX Port
17,18	LT, LC	Tuning Inductor
25,30	Gx1,Gx2	Tuning Capacitors for isolation
20,21	ANT	Antenna Port
27,28	RX	RX Port

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, Tcase=+85°C, 800MHz	TX, ANT	80	W
RF Input Power Peak, Tcase=+85°C, 800MHz, 10% duty cycle, 10msec pulse width	TX, ANT	400	W
RF Input Power CW, Tcase=+85°C, 2.6GHz	TX, ANT	70	W
RF Input Power Peak, Tcase=+85°C, 2.6GHz, 1% duty cycle, 10usec pulse width	TX, ANT	500	W
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	4.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		700		2700	MHz
Insertion loss, TX	800MHz		0.40	0.55	dB
	1400MHz		0.50		
	2600MHz		0.65		
Insertion loss, RX	800MHz		0.75	0.90	dB
	1400MHz		0.90		
	2600MHz		1.00		
Isolation ANT-TX	800MHz	17	22		dB
	1400MHz		25		
	2600MHz		27		
Isolation ANT-RX	800MHz	45	50		dB
	1400MHz		50		
	2600MHz		55		
Return Loss RX (TX)	800MHz		25 (20)		dB
	1400MHz		20 (18)		
	2600MHz		27 (25)		
H2	800MHz, Pin=35dBm		-70		dBc
H3	800MHz, Pin=35dBm		-75		dBc
IIP3	800MHz		60		dBm
P0.1dB CW	0.1dB compression point, 800MHz		100		W
P0.1dB Peak	Duty Cycle 1% with 10usec pulse width, 800MHz		631		W
P0.1dB Peak	Duty Cycle 15% with 1.5msec pulse width, 800MHz		450		W
P0.1dB CW	0.1dB compression point, 2600MHz		90		W
P0.1dB Peak	Duty Cycle 1% with 10usec pulse width, 2600MHz		550		W
Switching time	50% ctrl to 10/90% of the RF value is settled. CP=1nF to ground on VCP pin.		2.2		μs
Control voltage	Power Supply VDD	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current consumption, IDD	Active mode (VDD on)		160	200	μA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	Active RF Path
0	ANT-RX
1	ANT-TX

Attention:
[1] VDD should be applied first before V1, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on V1 control pin, the state at start-up without any control voltage applied will be ANT-RX.

9.0 Evaluation Board

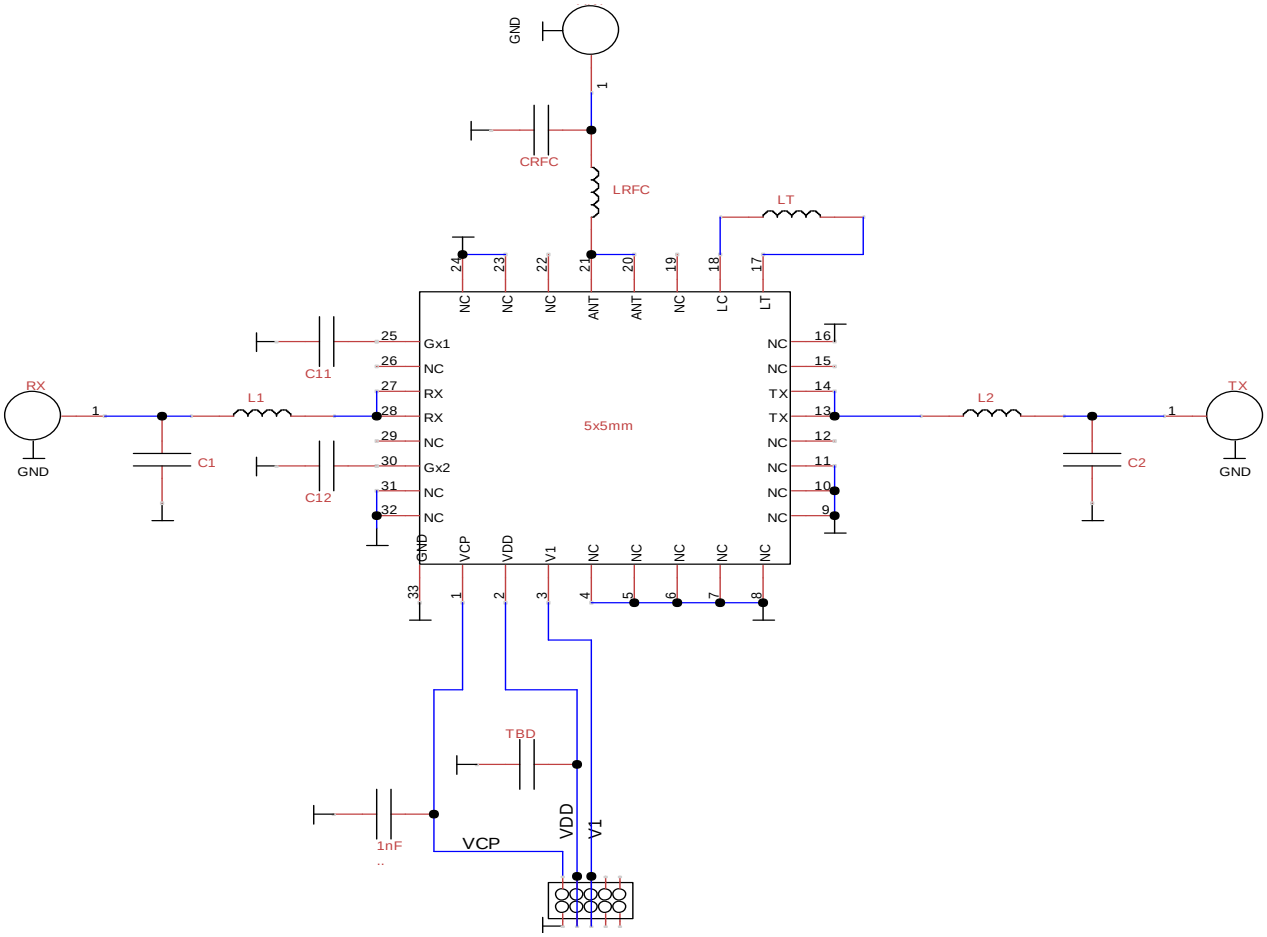


Figure 3 Evaluation Board Schematic

Attention:
[1] **33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be added.**
[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

Table 6 Matching components for various frequency bands

Freq	LT	LRFC	L1	L2	CRFC	C1	C2	C11	C12	CP
0.8 – 1GHz	**47nH**	**Short**	**Short**	**Short**	**Open**	**Open**	**Open**	**8.2pF**	**8.2pF**	**1nF**
0.9 - 1.1GHz	**36nH**	**Short**	**Short**	**Short**	**Open**	**Open**	**Open**	**8.2pF**	**8.2pF**	**1nF**
1.2 - 1.4GHz	**27nH**	**Short**	**Short**	**Short**	**Open**	**Open**	**Open**	**8.2pF**	**8.2pF**	**1nF**
2.3 – 2.7GHz	**5.6nH**	**1.0nH**	**1.0nH**	**1.0nH**	**0.5pF**	**0.4pF**	**0.7pF**	**1.7pF**	**1.7pF**	**1nF**

Inductos : ATC 0402WL or Coilcraft 0402HP series, Capacitors : Passive Plus 0603N series

10.0 Typical Characteristics (Tune 1.2 – 1.4Ghz Tune)

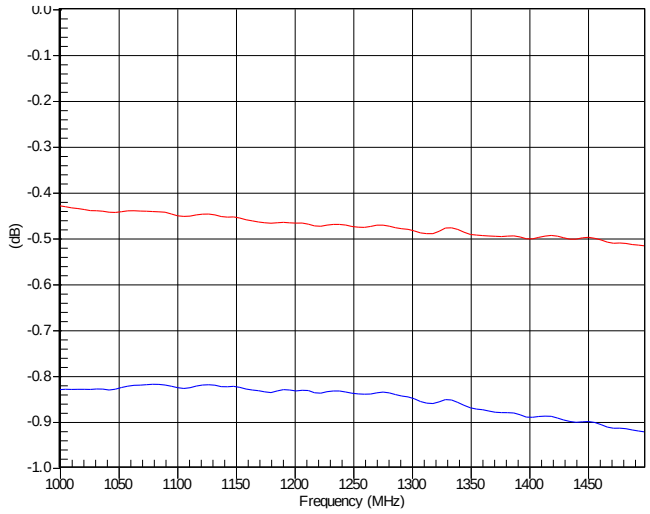


Figure 4 TX (Red), RX (Blue) Insertion Loss

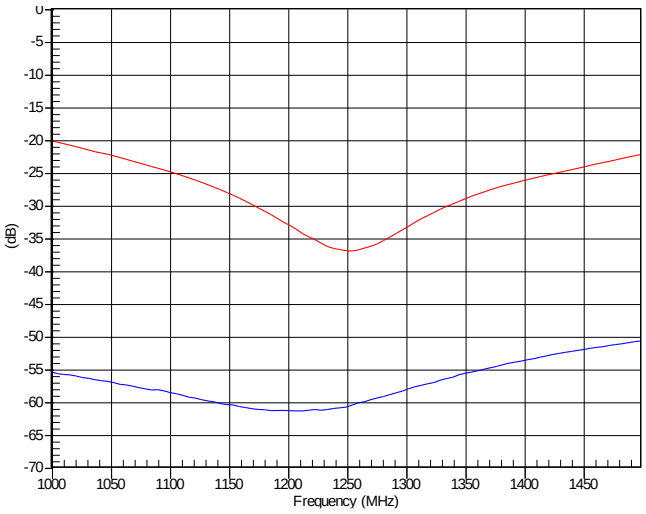


Figure 5 TX (Red), RX (Blue) Isolation

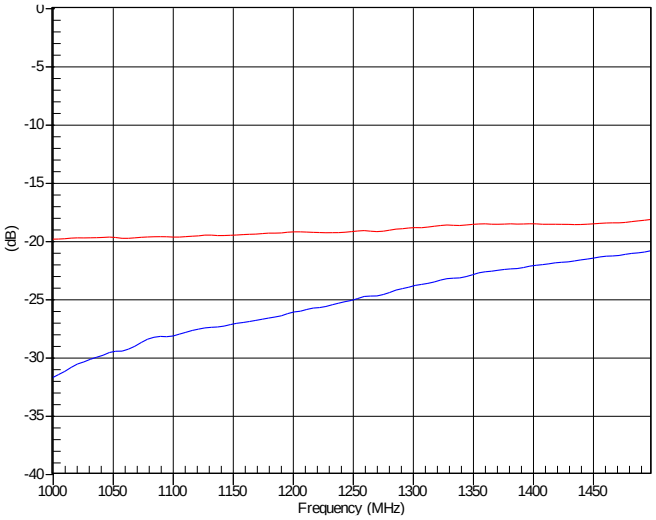


Figure 6 TX (Red), RX (Blue) Return Loss

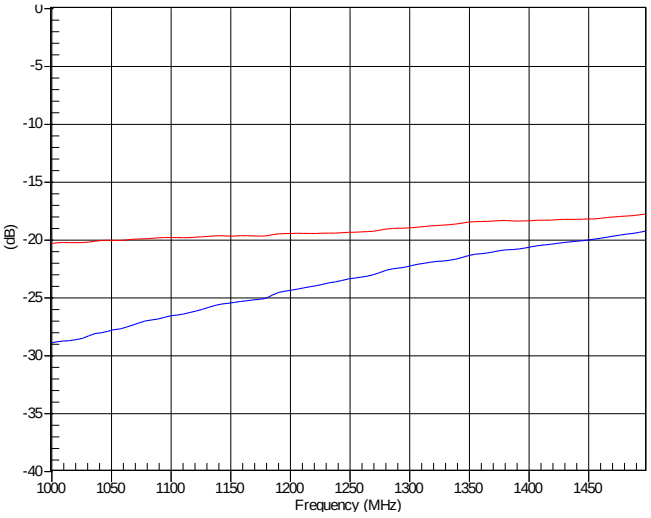


Figure 7 TX (Red), RX (Blue) ANT Return Loss

11.0 Typical Characteristics (Tune 2.3 – 2.7Ghz Tune)

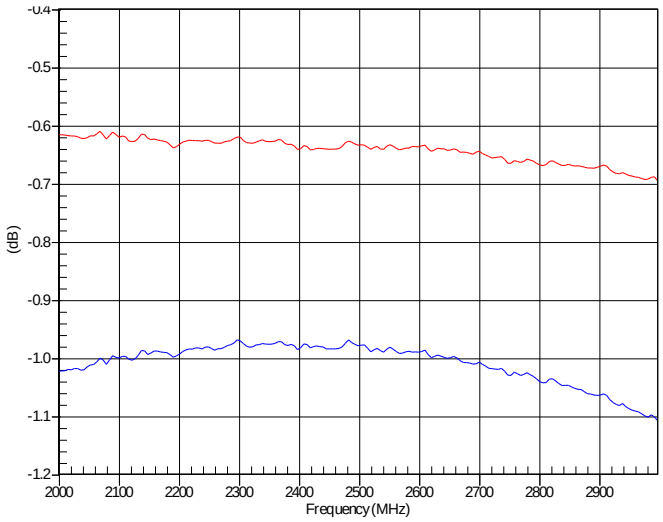


Figure 8 TX (Red), RX (Blue) Insertion Loss

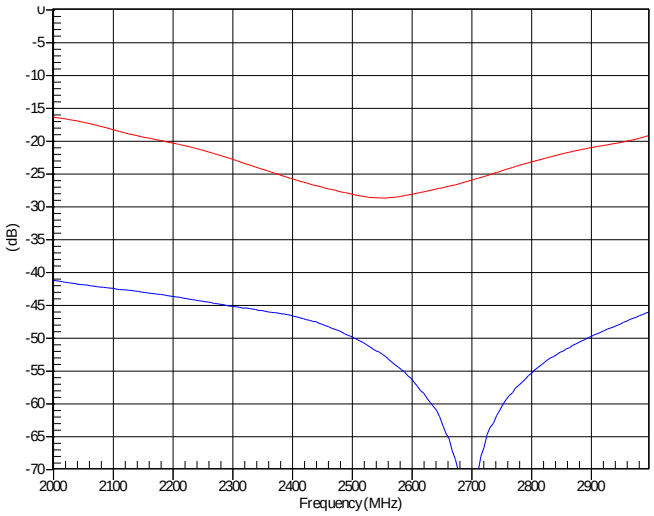


Figure 9 TX (Red), RX (Blue) Isolation

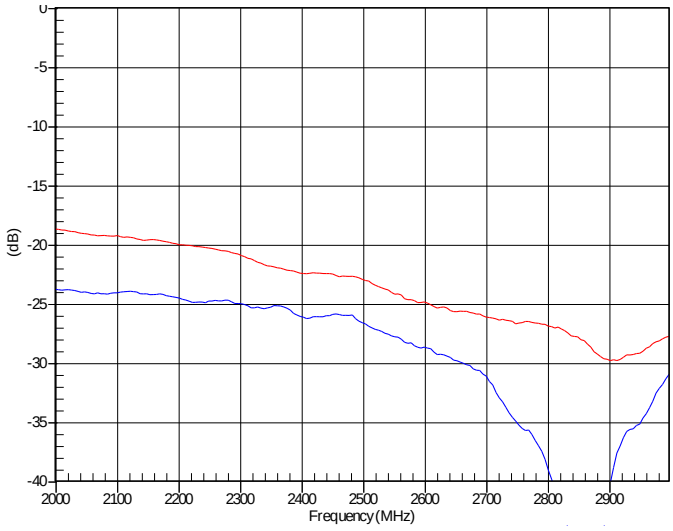


Figure 10 TX (Red), RX (Blue) Return Loss

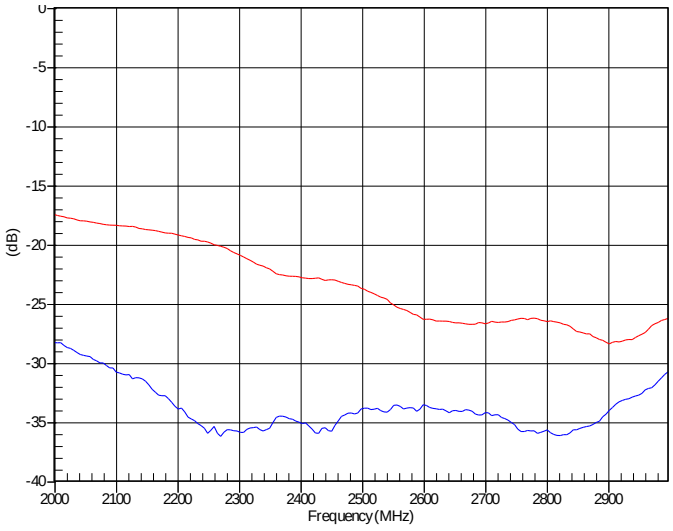


Figure 11 TX (Red), RX (Blue) ANT Return Loss

12.0 Device Package Information

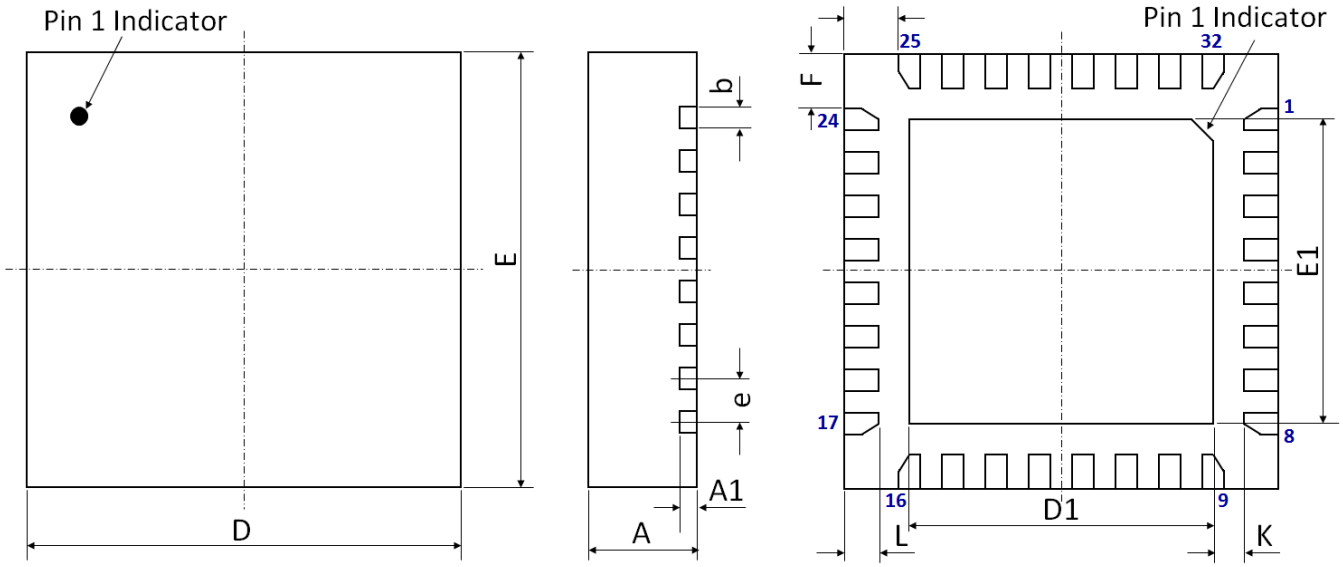


Figure 12 Device Package Drawing
(All dimensions are in mm)

Table 7 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.85	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.10	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.10	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.50	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com for PCB and soldering related guidelines.

13.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 5(X)×5(Y)=25.

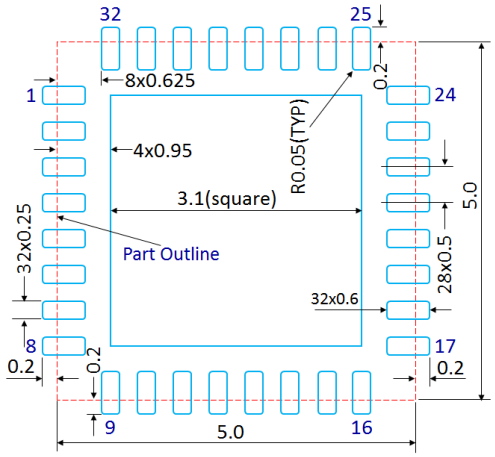
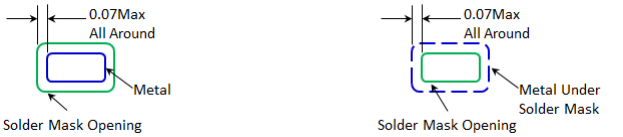


Figure 13 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 14 Solder Mask Pattern
(Dimensions are in mm)

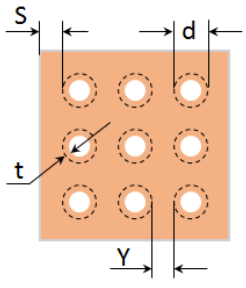


Figure 15 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

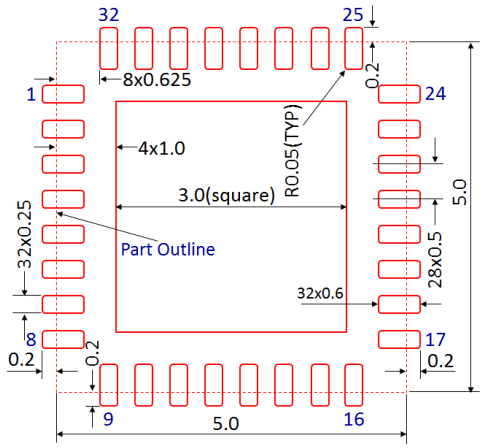


Figure 16 Stencil Openings
(Dimensions are in mm)

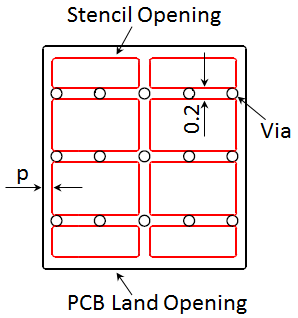


Figure 17 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

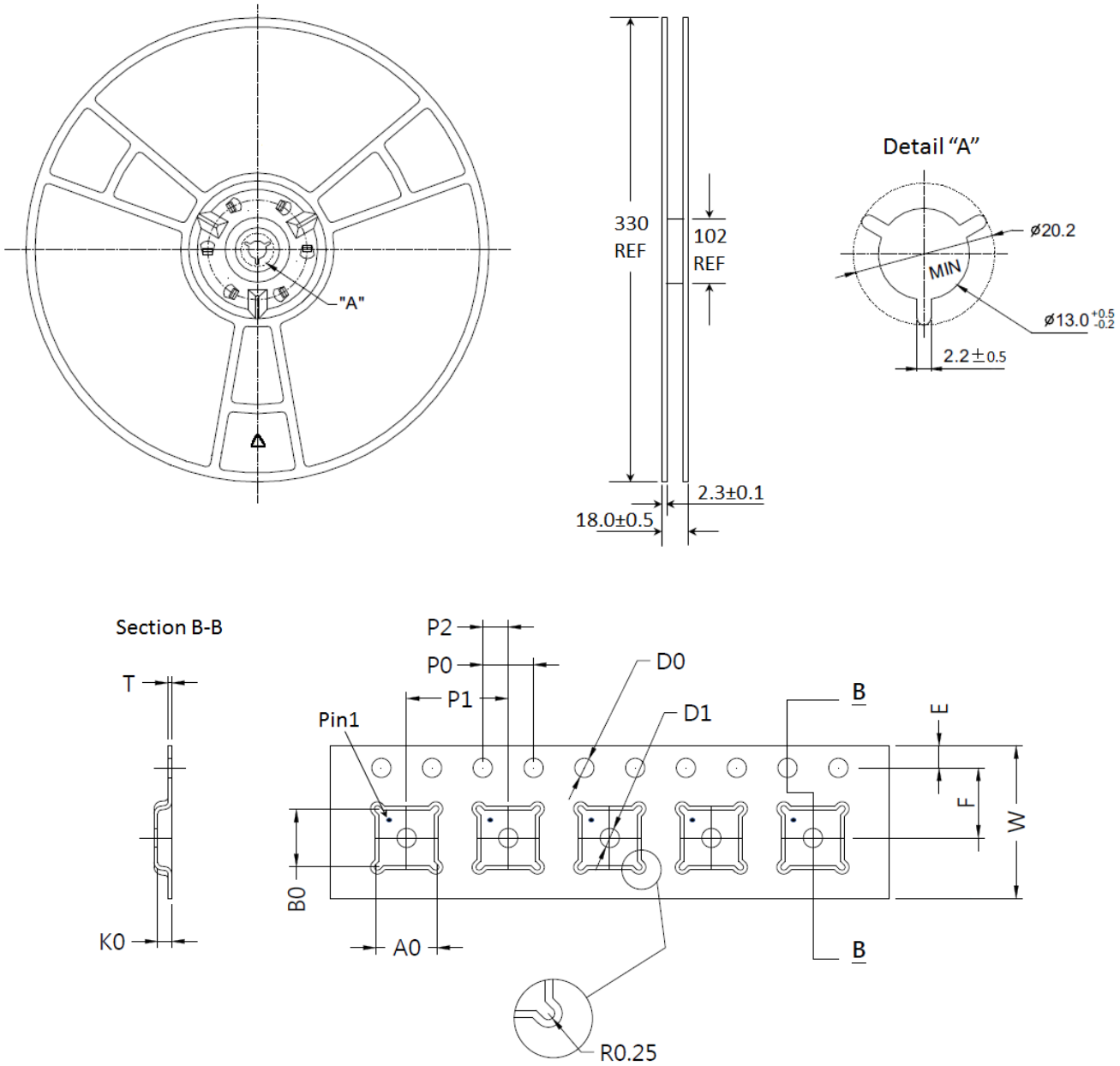


Figure 18 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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